IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Robert J. Schultz
Group Art Unit: 2419

Application No.: 10/809,164
Examiner: Choi, Eunsook

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For: PROCESSING PACKET INFORMATION USING AN ARRAY OF PROCESSING ELEMENTS

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated March 9, 2009, which finally rejected claims 1-15, 17, 18, 20, and 21 in the above-identified application. The Office date of receipt of Appellant's Notice of Appeal was June 9, 2009. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

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Date:_____ Signed:_____

Typed Name: Mark A. Wilson

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, Riverstone Networks, Inc., of Santa Clara, California.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF CLAIMS

Claim 19 is canceled.

No claims are withdrawn.

Claim 16 was objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-15, 17, 18, 20, and 21 stand rejected as follows:

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Key et al. (U.S. Pat. No. 6,272,621, hereinafter Key) in view of Rhoades et al. (U.S. Pat. Pub. No. 2003/0041163, hereinafter Rhoades).

Claims 1, 2, and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhoades in view of Van Lunteren et al. (U.S. Pat. No. 7,193,997, hereinafter Van Lunteren).

Claims 6, 7, 11, 14, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Key in view of Rhoades and Van Lunteren.

Claims 13, 17, 18, 20, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Key in view of Rhoades and Kaganoi et al. (U.S. Pat. Pub. No. 2003/0012198, hereinafter Kaganoi).

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhoades modified by Van Lunteren and further in view of Khanna (U.S. Pat. No. 7,219,187, hereinafter Khanna).

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Key modified by Rhoades and Van Lunteren and further in view of Khanna.

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Key modified by Rhoades and Van Lunteren and further in view of Kaganoi.

Claims 1-15, 17, 18, 20, and 21 are the subject of this appeal. A copy of claims 1-15, 17, 18, 20, and 21 is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

There were no proposed amendments submitted subsequent to the Final Office Action mailed March 9, 2009.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This section of this Appeal Brief is set forth to comply with the requirements of 37 C.F.R. § 41.37(c)(1)(v) and is not intended to limit the scope of the claims in any way. Examples of implementations of the limitations of independent claims 1, 6, 12, and 18 are described below.

The language of claim 1 relates to a method for processing packet information using an array of processing elements. Page 3, paragraph 8, lines 1-2. The method includes performing a first search using a first stage processing element related to a packet using first search information. Page 3, paragraph 9, lines 8-10. The method also includes performing, in parallel with the first search, search-independent processing using a second stage processing element on information related to the packet. Page 3, paragraph 9, lines 8-10. The method also includes performing search-dependent processing using a result from the first search and a result of the search-independent processing to produce second search information. Page 3, paragraph 8, lines 6-8.

The language of claim 6 relates to a method for processing packet information. The method includes processing information related to a packet using a first stage processing element to produce a first search key. Page 6, paragraph 23, lines 19-22. The first stage processing element is included within an array of processing elements. Page 6,

paragraph 23, lines 14-15. The method also includes searching a first stage memory unit using the first search key. Page 6, paragraph 23, lines 20-21. The method also includes performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage processing element. Page 6, paragraph 23, lines 26-28. The second stage processing element is included within the array of processing elements. Page 6, paragraph 23, lines 23-24. The method also includes performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key. Page 6, paragraph 23, lines 26-29. The method also includes searching a second stage memory unit using the second search key. Page 7, paragraph 23, lines 8-13.

The language of claim 12 relates a system for processing packet information. The system includes an array of processing elements. Page 6, paragraph 23, lines 1-2. The array of processing elements includes at least one first stage processing element. Page 6, paragraph 23, lines 17-18. The array of processing elements also includes at least one second stage processing element. Page 6, paragraph 23, lines 26-27. The system also includes a first stage memory unit that is searched in response to search information from the first stage processing element. Page 6, paragraph 23, lines 19-22. The first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet. Page 6, paragraph 23, lines 26-29.

The language of claim 18 relates to a system for processing packet information which includes an array of processing elements. Page 6, paragraph 23, lines 1-2. The array of processing elements includes a plurality of first stage processing elements. Page 4, paragraph 17, lines 10-13. The array of processing elements also includes a plurality of second stage processing elements. Page 4, paragraph 23, lines 10-13. The system also includes a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements and to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Page, 8, paragraph 26, lines 25-27. The first and second stage

processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets. Page 6, paragraph 23, lines 26-29.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claim 12 is patentable over the combination of Key and Rhoades under 35 U.S.C. 103(a).

B. Whether claims 1, 2, and 3 are patentable over the combination of Rhoades and Van Lunteren under 35 U.S.C. 103(a).

C. Whether claims 6, 7, 11, 14, and 15 are patentable over the combination of Key, Rhoades, and Van Lunteren under 35 U.S.C. 103(a).

D. Whether claims 13, 17, 18, 20, and 21 are patentable over the combination of Key, Rhoades, and Kaganoi under 35 U.S.C. 103(a).

E. Whether claims 4 and 5 are patentable over the combination of Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a).

F. Whether claim 10 is patentable over the combination of Key, Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a).

G. Whether claims 8 and 9 are patentable over the combination of Key, Rhoades, Van Lunteren, and Kaganoi under 35 U.S.C. 103(a).

VII. ARGUMENT

For the purposes of this appeal, claim 12 is argued separately for purposes of the question of patentability over combination of Key and Rhoades under 35 U.S.C. 103(a). Claims 1, 2, and 3 are argued together as a separate group for purposes of the question of patentability over the combination of Rhoades and Van Lunteren under 35 U.S.C. 103(a). Claims 6, 7, 11, 14, and 15 are argued together as a separate group for purposes of the question of patentability over the combination of Key, Rhoades, and Van Lunteren under 35 U.S.C. 103(a). Claims 13, 17, 18, 20, and 21 are argued together as a separate group for purposes of the question of patentability over the combination of Key, Rhoades, and Kaganoi under 35 U.S.C. 103(a). Claims 4 and 5 are argued together as a separate group

for purposes of the question of patentability over the combination of Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a). Claim 10 is argued separately for purposes of the question of patentability over the combination of Key, Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a). Claims 8 and 9 are argued together as a separate group for purposes of the question of patentability over the combination of Key, Rhoades, Van Lunteren, and Kaganoi under 35 U.S.C. 103(a).

A. Claim 12 is patentable over the combination of Key and Rhoades because the combination of cited references does not teach all of the limitations of the claim.

Appellant respectfully submits that claim 12 is patentable over the combination of Key and Rhoades because the combination of references does not teach all the limitations of the claim. Claim 12 recites:

> A system for processing packet information comprising:
> an array of processing elements having;
> at least one first stage processing element; and
> at least one second stage processing element; and
> a first stage memory unit that is searched in response to search information from the first stage processing element;
> wherein the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet.
> (Emphasis added.)

Claim 12 is patentable over the combination of Key and Rhoades for at least two reasons. First, the Examiner does not establish a *prima facie* rejection based on the combination of Key and Rhoades because the Examiner does not provide articulated reasoning with some rational underpinning to address the "same packet" language of the claim. Second, the combination of Key and Rhoades does not teach a second stage processing element that performs search-independent processing in parallel to the first stage processing unit.

1. The Examiner does not establish a *prima facie* rejection based on the combination of Key and Rhoades because the Examiner does not provide articulated reasoning with some rational underpinning to address the "same packet" language of the claim.

The Examiner does not establish a *prima facie* rejection based on the combination of Key and Rhoades because the Examiner does not provide articulated reasoning with some rational underpinning to address the "same packet" language of the claim. In order to establish a *prima facie* rejection of a claim under 35 U.S.C. 103, the Office Action must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

For a proper contextual understanding, it should be noted that the "same packet" refers to the packet related to both 1) the search-independent processing of the second stage and 2) the search by the first stage of the first stage memory unit.

In contrast, the analysis presented in the Office Action for the rejection of claim 12 does not address a "same packet" that is related to both search-independent processing and a search of a first stage memory unit, as recited in the claim. In support of the rejection, the Examiner states in the Office Action that:

> Rhoades teaches in Fig. 8, **Perform Table Lookup** (a search of a first stage memory unit) is processed in parallel with **Transmission Error Detection – Packet Lifetime Calculations** (a second stage processing element, to allow a second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit.) Rhoades teaches, further in detail, Fig. 14 table look up with internal/external RAM and [0083] adjacent PEs [processing elements] have close-coupled inter-processor communication paths that provide a low cost means of sharing and aggregating the results from individual PEs simultaneously with the parallel processing itself, as shown in Fig. 8 of Rhoades.
>
> Office Action, 3/9/09, page 2.

While this referenced text from the Office Actions refers to some of the language of the claim, there is no reference within the indicated response from the Examiner to address the claim language related to the "same packet." Specifically, there is no explanation or analysis in the Office Action to attempt to show how the **Fig. 8, Perform Table Lookup** and the **Transmission Error Detection – Packet Lifetime Calculations** might operate with respect to the same packet. Moreover, although the text on page 4 of the Office Action acknowledges this claim language related to the "same packet," the analysis provided on page 4 of the Office Action also fails to explain how the **Fig. 8, Perform Table Lookup** and the **Transmission Error Detection – Packet Lifetime Calculations** referred to in the Office Action might operate with respect to the same packet.

In light of this failure to address all of the limitations of the claim, the Examiner fails to establish a *prima facie* rejection of claim 12 under 35 U.S.C. 103. In fact, the Examiner continues to fail to meet the minimum requirements to establish a *prima facie* rejection of the claim because the Examiner does not present articulated reasoning with some rational underpinning to explain how the **Fig. 8, Perform Table Lookup** and the **Transmission Error Detection – Packet Lifetime Calculations** of Rhoades might relate to the "same packet," as recited in the claim. As a result of failing to address all of the language of the claim and establish a *prima facie* rejection, the burden of proof does not shift to Applicant. Rather, the burden of proof continues to rest with the Examiner to show how the cited references might teach all of the limitations of the claim. Accordingly, Applicant respectfully requests that the rejection of claim 12 under 35 U.S.C. 103(a) be withdrawn because the Examiner fails to establish a *prima facie* rejection.

2. The combination of Key and Rhoades does not teach a second stage processing element that performs search-independent processing in parallel to the first stage processing unit.

The combination of Key and Rhoades does not teach a second stage processing element that performs search-independent processing in parallel to the first stage processing unit. Although the Examiner asserts that Rhoades

purportedly teaches this limitation, the Examiner's assertions fail to recognize that a table lookup is not search-independent processing as recited in the claim. In support of the rejection, the Examiner states in the Office Action that:

> However, Key does not expressly teach the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet. Rhodes teaches in Fig. 8, **Perform Table Lookup** is processed in parallel with **Transmission Error Detection – Packet Lifetime Calculations**.
> Office Action, 3/9/09, page 4.

While Fig. 8 of Rhoades shows a table lookup being performed in parallel with other operations, Rhoades does not teach that the table lookup is a search-independent operation. Rhoades cannot teach that the table lookup is a search-independent operation because a table lookup is in fact a search operation. Performing the table lookup in parallel with the other processes of a packet processor does not make the table lookup a search-independent operation.

Therefore, the combination of Key and Rhoades does not teach all of the limitations of claim 12 because the table lookup shown in Fig. 8 of Rhoades is not a search-independent operation. Accordingly, Appellant respectfully asserts independent claim 12 is patentable over the combination of Key and Rhoades because the combination of Key and Rhoades does not teach all of the limitations of the claim.

B. Claims 1, 2, and 3 are patentable over the combination of Rhoades and Van Lunteren because the combination of cited references does not teach all of the limitations of the claims.

Claims 1, 2, and 3 are patentable over the combination of Rhoades and Van Lunteren because the combination of cited references does not teach all of the limitations of the claims. Claim 1 recites:

A method for processing packet information using an array of processing elements comprising:

performing a first search using a first stage processing element related to a packet using first search information;

performing, in parallel with the first search, search-independent processing using a second stage processing element on information related to the packet; and

performing search-dependent processing using a result from the first search and a result of the search-independent processing to produce second search information.

(Emphasis added.)

Appellant respectfully asserts independent claim 1 is also patentable over the combination of Rhoades and Van Lunteren for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12. Although the language of claim 1 differs from the language of claim 12, and the scope of each claim should be interpreted independently of other claims, Appellant respectfully asserts that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of claim 1. Accordingly, Appellant respectfully asserts independent claim 1 is patentable over the combination of Rhoades and Van Lunteren because the combination of references does not teach the indicated limitations.

Given that claims 2 and 3 depend from and incorporate all of the limitations of the corresponding independent claim 1, which is patentable over the combination of Rhoades and Van Lunteren, Appellant respectfully submits that dependent claims 2 and 3 are also patentable over the cited references based on an allowable base claim. Additionally, each of claims 2 and 3 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 1, 2, and 3 under U.S.C 103(a) be withdrawn.

C. Claims 6, 7, 11, 14, and 15 are patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of cited references does not teach all of the limitations of the claims.

Appellant respectfully submits that claim 6 is patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of references does not teach all of the limitations of the claim. Claim 6 recites:

A method for processing packet information comprising:

processing information related to a packet using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements;

searching a first stage memory unit using the first search key;

performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage processing element, wherein the second stage processing element is included within the array of processing elements;

performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and

searching a second stage memory unit using the second search key.

(Emphasis added.)

Appellant respectfully asserts independent claim 6 is also patentable over the combination of Key, Rhoades, and Van Lunteren for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12. Although the language of claim 6 differs from the language of claim 12, and the scope of each claim should be interpreted independently of other claims, Appellant respectfully asserts that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of independent claim 6. Accordingly, Appellant respectfully asserts independent claim 6 is patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of Key, Rhoades, and Van Lunteren does not teach the indicated limitations.

Given that claims 7, 11, 14, and 15 depend from and incorporate all of the limitations of the corresponding independent claims 6 and 12, which are patentable over the combination of Key, Rhoades, and Van Lunteren, Appellant respectfully submits that dependent claims 7, 11, 14, and 15 are also patentable over the cited references based on an allowable base claim. Additionally, each of claims 7, 11, 14, and 15 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 6, 7, 11, 14, and 15 under U.S.C 103(a) be withdrawn.

D. Claims 13, 17, 18, 20, and 21 are patentable over the combination of Key, Rhoades, and Kaganoi because the combination of cited references does not teach all of the limitations of the claims.

Appellant respectfully submits that claim 18 is patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of references does not teach all of the limitations of the claim. Claim 18 recites:

> A system for processing packet information comprising:
> an array of processing elements having;
> a plurality of first stage processing elements; and
> a plurality of second stage processing elements; and
> a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements and to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, wherein the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets.
> (Emphasis added.)

Appellant respectfully asserts independent claim 18 is also patentable over the combination of Key, Rhoades, and Kaganoi for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12. Although the language of claim 18 differs from the language of claim 12, and the scope of each claim should be interpreted independently of other claims, Appellant respectfully asserts that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of independent claim 18. Accordingly, Appellant respectfully asserts independent claim 18 is patentable over the combination of Key, Rhoades, and Kaganoi because the combination of Key, Rhoades, and Kaganoi does not teach the indicated limitations.

Given that claims 13, 17, 20, and 21 depend from and incorporate all of the limitations of the corresponding independent claims 12 and 18, which are patentable over the combination of Key, Rhoades, and Kaganoi, Appellant respectfully submits that dependent claims 13, 17, 20, and 21 are also patentable over the cited references based on allowable base claims. Additionally, each of claims 13, 17, 20, and 21 may be allowable

for further reasons. Accordingly, Appellant requests that the rejections of claims 13, 17, 18, 20, and 21 under U.S.C 103(a) be withdrawn.

E. Claims 4 and 5 are patentable over the combination of Rhoades, Van Lunteren, and Khanna because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 4 and 5 depend from and incorporate all of the limitations of the corresponding independent claim 1, which are patentable over the combination of Rhoades, Van Lunteren, and Khanna, Appellant respectfully submits that dependent claims 4 and 5 are also patentable over the cited references based on an allowable base claim. Additionally, each of claims 4 and 5 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 4 and 5 under U.S.C 103(a) be withdrawn.

F. Claim 10 is patentable over the combination of Key, Rhoades, Van Lunteren, and Khanna because the combination of cited references does not teach all of the limitations of the claim.

Given that claim 10 depends from and incorporates all of the limitations of the corresponding independent claim 6, which is patentable over the combination of Key, Rhoades, Van Lunteren, and Khanna, Appellant respectfully submits that dependent claim 10 is also patentable over the cited references based on an allowable base claim. Additionally, claim 10 may be allowable for further reasons. Accordingly, Appellant requests that the rejection of claim 10 under U.S.C 103(a) be withdrawn.

G. Claims 8 and 9 are patentable over the combination of Key, Rhoades, Van Lunteren, and Kaganoi because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 8 and 9 depend from and incorporate all of the limitations of the corresponding independent claim 6, which is patentable over the combination of Key, Rhoades, Van Lunteren, and Kaganoi, Appellant respectfully submits that dependent claims 8 and 9 are also patentable over the cited references based on an allowable base

claim. Additionally, claims 8 and 9 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 8 and 9 under U.S.C 103(a) be withdrawn.

VIII. CONCLUSION

For the reasons stated above, claims 1-15, 17, 18, 20, and 21 are patentable over the cited references. Thus, the rejections of claims 1-15, 17, 18, 20, and 21 should be withdrawn. Appellant respectfully requests that the Board reverse the rejections of claims 1-15, 17, 18, 20, and 21 under 35 U.S.C. 103(a) and, since there are no remaining grounds of rejection to be overcome, direct the Examiner to enter a Notice of Allowance for claims 1-15, 17, 18, 20, and 21.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. A method for processing packet information using an array of processing elements comprising:

performing a first search using a first stage processing element related to a packet using first search information;

performing, in parallel with the first search, search-independent processing using a second stage processing element on information related to the packet; and

performing search-dependent processing using a result from the first search and a result of the search-independent processing to produce second search information.

2. The method of claim 1 further including performing a second search using the second search information.

3. The method of claim 2 further including holding a processing state from the search-independent processing until the result from the first search is available.

4. The method of claim 2 wherein performing search-dependent processing to produce the second search information includes producing a comparand and a mask as the second search information.

5. The method of claim 4 wherein performing the second search includes searching a content addressable memory using the comparand and the mask.

6. A method for processing packet information comprising:

processing information related to a packet using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements;

searching a first stage memory unit using the first search key;

performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage

processing element, wherein the second stage processing element is included within the array of processing elements;

performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and

searching a second stage memory unit using the second search key.

7. The method of claim 6 further including holding a processing state from the search-independent processing until the result from the search of the first stage memory unit is received at the second stage processing element.

8. The method of claim 7 further including providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit.

9. The method of claim 6 further including providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit.

10. The method of claim 6 wherein the first and second search keys include a comparand and a mask.

11. The method of claim 6 further including forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced.

12. A system for processing packet information comprising:

an array of processing elements having;

at least one first stage processing element; and

at least one second stage processing element; and

a first stage memory unit that is searched in response to search information from the first stage processing element;

wherein the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet.

13. The system of claim 12 further including a direct communications link between the first stage memory unit and the second stage processing element configured to provide search results directly to the second stage processing element from the first stage memory unit.

14. The system of claim 12 wherein the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key.

15. The system of claim 14 further including a second stage memory unit that is associated with the second stage processing element, wherein the search key is used to search the second stage memory unit.

16. The system of claim 15 further including at least one third stage processing element, wherein the second and third stage processing elements are configured to allow the third stage processing element to perform search-independent processing related to the packet in parallel with the search of the second stage memory unit.

17. The system of claim 12 wherein the first stage memory unit comprises content addressable memory.

18. A system for processing packet information comprising:

an array of processing elements having;

a plurality of first stage processing elements; and

a plurality of second stage processing elements; and

a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements and to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, wherein the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets.

19. (canceled)

20. The system of claim 18 wherein the first stage processing elements forward information to respective second stage processing elements before results from respective searches of the first stage memory unit are received by the second stage processing elements.

21. The system of claim 18 further including:

a first bus that connects the plurality of first stage processing elements to the memory interface; and

a second bus that connects the plurality of second stage processing elements to the memory interface.

X. EVIDENCE APPENDIX

There is no evidence submitted with this Appeal Brief.

XI. RELATED PROCEEDINGS APPENDIX

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.